Serial No.: 10/791,096
Group Art Unit: 2813

AMENDMENTS TO CLAIMS

- Please delete claims 3, 8, 13, and 18.
- Please amend pending claims 1, 2, 6, 11, and 17 as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;
forming a gate on the gate dielectric;
forming source/drain junctions in the semiconductor substrate;
forming a silicide on the source/drain junctions and on the gate within a thermal budget having a temperature dependent upon a silicide metal;
depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;
forming contact liners in the contact holes within the thermal budget for forming the silicide; and
forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

2. (currently amended) The method as claimed in claim 1 wherein:
forming the ~~tungsten nitride~~ contact liners uses an atomic layer deposition process.

3. (cancelled)

4. (original) The method as claimed in claim 1 wherein:
forming the silicide forms a nickel silicide.

5. (original) The method as claimed in claim 1 wherein:
forming the contacts forms a tungsten material; and
forming the contact liners forms a tungsten nitride material.

6. (currently amended) A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a nickel silicide on the source/drain junctions and on the gate within a thermal budget having a temperature of less than about 400 degrees centigrade;

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming tungsten nitride contact liners in the contact holes within the thermal budget for forming the nickel silicide; and

forming tungsten contacts in the contact holes over the contact liners.

7. (original) The method as claimed in claim 6 wherein:

forming the tungsten nitride contact liners uses an atomic layer deposition process.

8. (cancelled)

9. (original) The method as claimed in claim 6 wherein:

forming the nickel silicide uses an ultra-thin thickness of a nickel silicide metal.

10. (original) The method as claimed in claim 6 wherein:

depositing the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

11. (currently amended) An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

an ultra-thin silicide on the source/drain junctions and on the gate;

an interlayer dielectric having contact holes therein above the semiconductor substrate;

contact liners in the contact holes; and

contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

12. (original) The integrated circuit as claimed in claim 11 wherein:
the silicide is a nickel silicide.

13. (cancelled)

14. (original) The integrated circuit as claimed in claim 11 wherein:
the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

15. (original) The integrated circuit as claimed in claim 11 wherein:
the contacts in the contact holes are materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

16. (original) The integrated circuit as claimed in claim 11 wherein:
the contacts are a tungsten material; and
the contact liners are a tungsten nitride material.

17. (currently amended) An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
source/drain junctions in the semiconductor substrate;
an ultra-thin thickness of a nickel silicide on the source/drain junctions and on the gate,
an interlayer dielectric having contact holes therein above the semiconductor substrate;
tungsten nitride contact liners in the contact holes; and
tungsten contacts in the contact holes over the contact liners.

18. (cancelled)

19. (original) The integrated circuit as claimed in claim 17 wherein:
the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

20. (original) The integrated circuit as claimed in claim 17 wherein:
the nickel silicide further comprises arsenic doping.